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# Design and Performance Assessment of an Airborne Ice Sounding Radar Front-End

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**Abstract**— The paper describes the design and experimental performance assessment of the RF front-end of an airborne P-band ice sounding radar. The ice sounder design features newly developed components at a centre frequency of 435 MHz, such as, antenna 20% bandwidth at RL < 13 dB, compact high power in-phase and out-of-phase power dividers with a relative bandwidth of 20% and more than 75W CW power handling, high power SPDT PIN switch with 90W CW power handling and a 70W CW High efficiency LDMOS power amplifier with >60% power-added efficiency. The system comprises also a digital signal generator, a digital front-end and a control unit. The system was functionally tested in March 2008 and had a first successful proof-of-concept campaign in Greenland in May 2008.

special care is taken to achieve good calibration and stability [2].

## I. INTRODUCTION

The European Space Agency has assigned the Technical University of Denmark (DTU) the development of an airborne P-band ice sounding radar demonstrator, hereinafter the “P-sounder”. The project will help to understand the behavior of ice at P-band and it will enable the detection of internal ice layers, reflection from the base of the ice sheet and validation of data processing algorithms for future satellite missions.

Key parameters of the instrument are listed in Table I and additional specifications and requirements are found in [1]. Fig. 1. shows the P-sounder installed on the Twin Otter aircraft.

TABLE I  
P-SOUNDER SPECIFICATIONS

Centre frequency	435 MHz
Bandwidth (goal)	85 MHz
Polarization	Quad
Maximum pulse length	50 $\mu$ s
Peak power	120 W
Maximum PRF	20 kHz
Operating altitude	3500 m

The system sensitivity is sufficient to detect the bedrock through 4 km of ice and pulse-to-pulse coherence helps improving the sensitivity. Surface clutter suppression is implemented with the help of synthetic aperture processing. The P-sounder features an experimental coherent clutter suppression capability based on a multiple-phase-centre antenna. The technique is similar to that of the MARSIS sounder [1]. Full polarimetry is justified by ice physics and

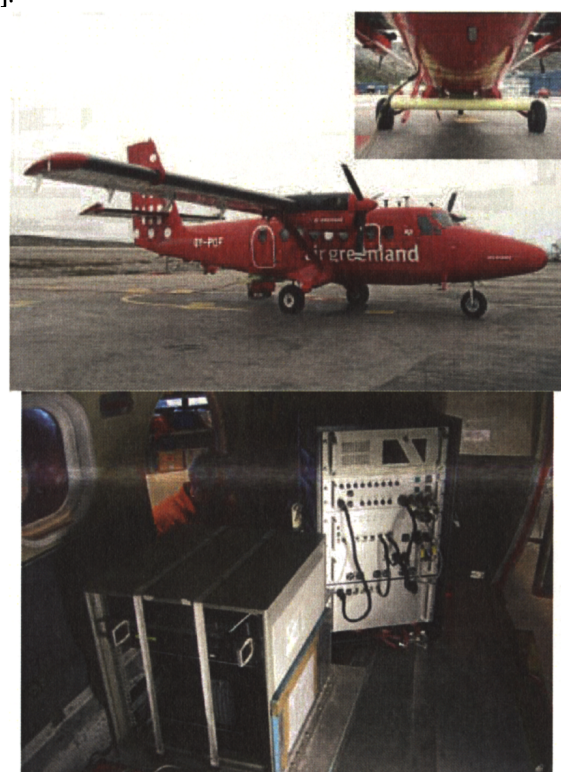


Fig. 1. Twin Otter aircraft with the antenna under the fuselage (left) and P-sounder system mounted inside (right).

A system analysis based on the envisioned flight geometry, system specifications, and data processing suggests that a peak power of 100 W in combination with an antenna with four patches in the across-track direction is sufficient to detect the bedrock down to 4 km. Based on very good experience with the airborne EMISAR system [3] the internal calibration is done by looping the generated pulses around as close to the antennas as possible and back through the receiver channel. This way the calibration is carried out in an almost perfect way by using exactly the same signal as used during normal operation.

The paper describes the design of the key RF components and shows preliminary measurements of the system. Additional

information about the newly developed wideband probe-fed dual-linear polarisation wideband microstrip patch antenna array can be found in [4]. Both experimental results and simulations agree well in most cases for the individual components and the relative bandwidth requirement of >20% is realized with most components.

## II. RF FRONT-END COMPONENTS

The RF architecture is shown in Fig. 2. The transmitter is composed of a high power high-efficiency LDMOS amplifier, a high power SPDT PIN switch, a circulator, a slow high power relay for calibration and high power splitters. The receiver front-end is composed of a limiter, a low-noise amplifier, band pass filters and a variable gain amplifier that provides sufficient gain to drive optimally the A/D converters in the digital acquisition unit.

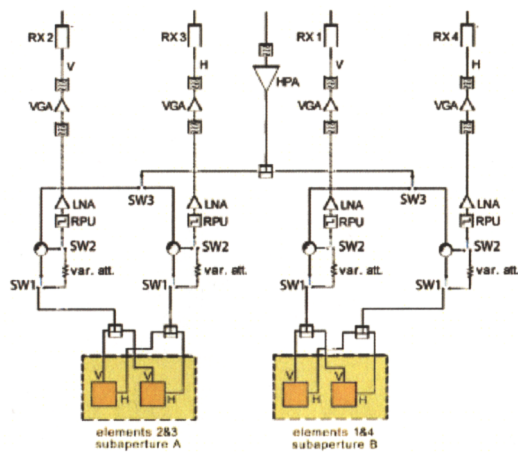


Fig. 2. RF Front-End architecture

### A. Power Dividers

We have developed lumped element Wilkinson type in-phase and out-of-phase power dividers. Such realizations have been presented earlier [5], [6], but did not have the RF power handling capabilities. Out-of-phase lumped element power dividers have also been reported earlier [7] including dividers using metamaterial lines [8]. The design here is based on metamaterial lines, but exhibits a better bandwidth performance and can handle higher powers with considerably less losses. Fig. 3 shows a photograph of the out-of-phase Wilkinson divider employing left-handed/right-handed sections to realize the  $180^\circ$  phase shift between the ports 2 and 3. The dimensions of both divider circuits are around  $60 \text{ mm} \times 40 \text{ mm}$ .

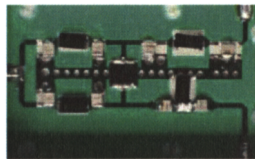


Fig. 3. Photograph of the fabricated  $180^\circ$  lumped element Wilkinson divider.

The design is a compromise between amplitude and phase unbalance. The phase difference between the ports has been adjusted to the very small value of around  $4^\circ$ , at the expense of an amplitude unbalance of 0.23 dB. The circuit inevitably exhibits higher losses as compared with the standard Wilkinson divider realized here (insertion loss 0.2 dB), but the measured losses remain below 0.5 dB, comparable to a  $180^\circ$  coupler. The phase difference has a maximum measured variation of  $2^\circ$ , which is an excellent value and matches perfectly  $180^\circ$  at the center frequency. Even better results, amplitude difference of 0.1 dB, insertion loss of 0.2 dB, phase balance  $< 1^\circ$  over the frequency band has been achieved for the in-phase lumped element Wilkinson divider. The necessary 20% bandwidth is realized for both circuits with a return loss better than 15 dB and power handling capabilities up to around 75 W CW microwave power.

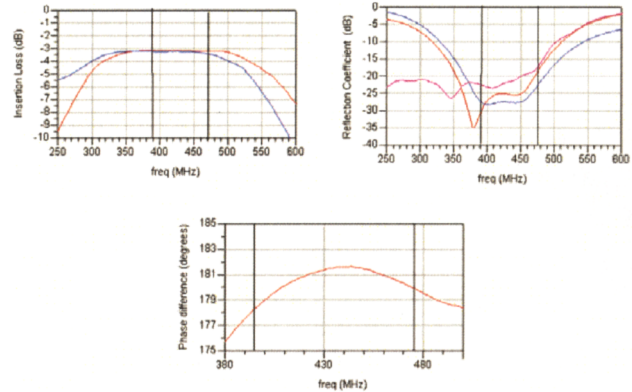


Fig. 4. Measured insertion loss, reflection coefficient and phase difference for the  $180^\circ$  Wilkinson divider.

### B. High Efficiency Power Amplifier

Solid-state high power amplifiers (HPA) with the required output peak power  $>100 \text{ W}$  and the bandwidth of 80 MHz at the frequency of operation are available from a very limited number of suppliers on a custom made basis and at a very high price. Therefore, we have developed a high efficiency power amplifier based on a proprietary design with 70 W CW output power, 0.1dB 395 – 475MHz bandwidth, high PAE of up to 68 % and with a 28 V bias voltage.

The design operates on class B and the series tuning is preferred over parallel tuning due to the low impedance levels. The design is based on two stages, a driver and a power stage. Both stages have been initially designed, fabricated and measured separately. Afterwards, the stages have been combined successfully and the final amplifier fabricated on a FR4 professional board is shown in Fig. 5.

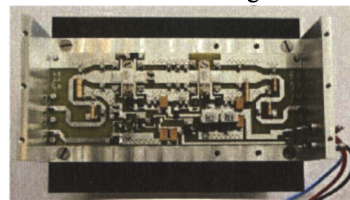


Fig. 5. High-efficiency power amplifier for P-Band (84x154x35 mm).

A comparison between measured and simulated transducer gain and input reflection for the final design indicate that our predictions are rather reliable, as indicated in Figure 6. Both measured parameters are in excellent agreement with simulated results using the Freescale LDMOS model. In the operating range of the radar the HPA exhibits an input return loss of > 11 dB and a total 38.9 dB gain. Measurements of the output power, efficiency and transducer gain are shown in table II for the frequencies of interest with 9.6dBm input power.

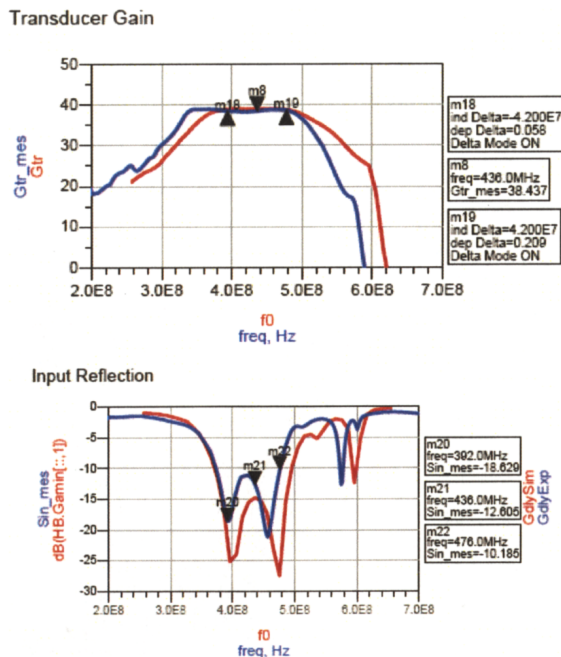


Fig. 6. Measured and simulated gain and return loss of the power amplifier.

TABLE III  
HPA MEASUREMENTS WITH 9.6dBm INPUT POWER.

Freq (MHz)	Power (W)	Eff. (%)	Gain (dB)
395	70.87	69.9	38.905
435	71.39	68.8	38.436
475	70.87	69.9	38.905

The radar front-end transmitter uses two of these power amplifiers modules in parallel to provide > 100W peak power. The bias of both amplifiers has been carefully adjusted to obtain amplifiers with equal gain at the cost of reducing the efficiency to 60%. The measured power at the output of the power combiner is 128.8 W CW at 435MHz. The gate of the power amplifiers can be switched on and off in order to improve the power dissipation capabilities and reduce the noise level generated during reception.

### C. High Power SPDT PIN Switch

Due to the lack of commercially available switches combining high power handling capabilities and a relatively high switching speed, a SPDT PIN switch driven by a fast

TTL control circuit has been developed. The design is shown in Fig. 7, where a physical separation between the two RF branches and the driven circuit ensures high isolation at high power levels. The topology selected allows a trade-off between insertion loss and isolation, and consists of two shunted PIN diodes in each branch separated by a  $\lambda/4$  lumped section [11]. Two PIN diode simulation models have been successfully used in ADS during the design stage: one to simulate the RF performance [12] and the other to predict the switching time [13]. Furthermore ultra fast MOSFET transistors and drivers have been used in the control circuit design. Fig. 8 shows that the measured return loss at the three ports is better than 15dB, the insertion loss is lower than 0.6dB and the isolation is better than 42.5 dB across the full band.

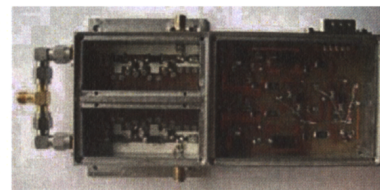


Fig. 7. RF PIN diode switch and fast driver circuit.

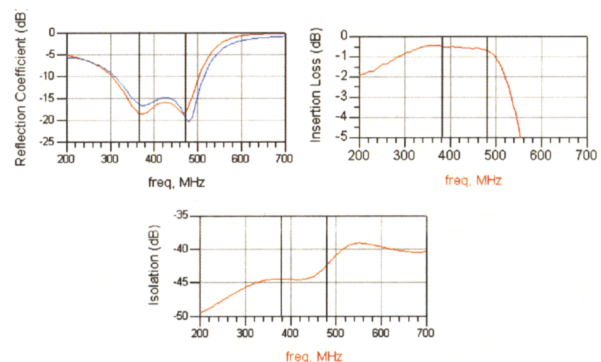


Fig. 8. Measured reflection coefficient, insertion loss, and isolation of the high power SPDT PIN switch.

The switching time measurements shown in Fig. 9. have been performed using a 435 MHz 90 W CW signal at the input. The measured delay time is 8  $\mu$ s, and it agrees well with the simulated values in Agilent ADS. The switch-on time is 500 ns and the switch-off time 300 ns. Furthermore, it is important to highlight that high voltage switching transients are not observed.

### D. System measurements

The receiver chain test results with a 435MHz -45dBm signal at the input of the LNA are shown in Fig. 10. It can be observed that the return loss is better than 25 dB and the overall gain of the receiver is programmed with the variable gain amplifier to be 41dB to drive the A/D converters optimally. The noise figure is deteriorated by the limiter placed in front of the LNA, but it is still lower than 2.6 dB. The PIN diode limiter is needed to protect the receiver during the transmission of high power pulses, and it also deteriorates the recovery time of the receiver. This is the time until the



receiver recovers its normal sensitivity after an overvoltage at the input of the limiter. Fig.11 shows the recovery time measured with an oscilloscope. The channel on the foreground is the result of combining a -45dBm CW signal and a pulsed signal that activates the limiter, and the channel on the background is the output of the receiver. It is possible to observe that the evolution of the receiver output is distorted during 800ns, but the time that the receiver is completely blind is only around 160ns.

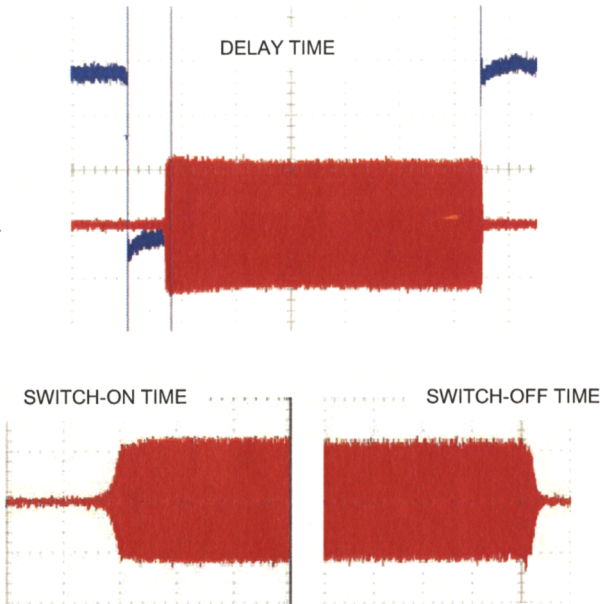


Fig. 9. Measured delay time (8  $\mu$ s), switch-on time (0.5  $\mu$ s) and switch-off time (0.3  $\mu$ s) of the high power SPDT PIN switch. (RF signal in red and TTL control signal in blue).

Other measurements and laboratory tests of the transmitter in combination with the digital signal generator will be shown during the presentation.

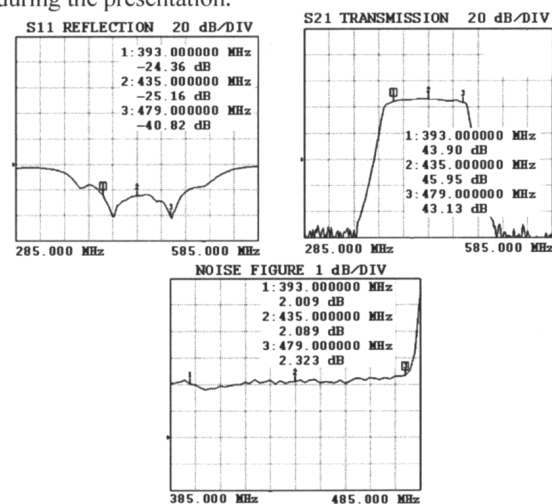


Fig. 10. Measured reflection coefficient, gain and noise figure of the receiver chain.

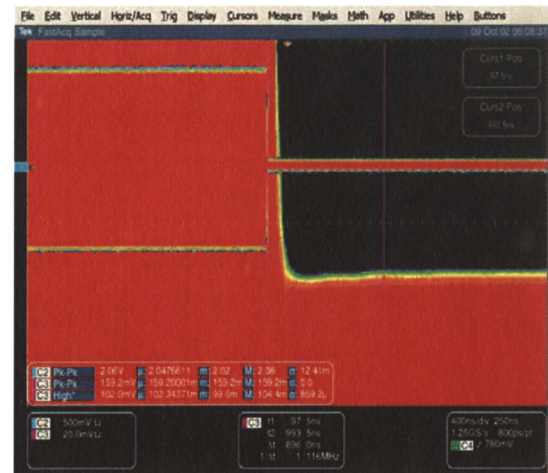


Fig. 11. Measured receiver recovery time (right)

### III. CONCLUSIONS

We have presented component design for a P-band ice sounding radar. The relative bandwidth of all components is around 20% at a return loss level of  $RL > 15$  dB. The RF components developed for the instrument are power dividers a high power amplifier and a high power SPDT PIN switch. Results for some of these components presented in the paper demonstrate the successful implementation of the design.

The lumped element Wilkinson dividers based on left-handed/right-handed sections presented in this paper exhibit wideband operation with low measured and simulated losses of  $< 0.5$  dB (0.2 dB for a standard lumped element Wilkinson divider) and good port matching. Phase unbalance between the ports in both circuits is  $4^\circ$  and  $2^\circ$ , respectively. All these results are maintained during high power operation up to the tested power levels of 75 W.

The HPA exhibits  $> 60\%$  PAE at 70 W output power over the required bandwidth. This performance is achieved by series matching to the low terminal impedances in class B operation. The driver stages and the narrowband version of the HPA both exhibit PAE approaching 70%. The driver and the HPA have good return loss and a constant gain across the frequency range. The driver gain varies only by 0.5 dB across the band and over the full power range. Excellent agreement is achieved between measurements and simulations in this case.

The high power SPDT PIN switch controlled by a 3.3V TTL input signal presents a return loss better than 15dB, an insertion loss lower than 0.6dB and an isolation  $> 42.5$  dB. The delay time is 8  $\mu$ s, the switch-on time 0.5  $\mu$ s and the switch-off time 0.3  $\mu$ s. A good agreement between the simulations using ADS and measurements was observed both for the RF design and the fast driver performance. Power handling capability up to 90 W CW was tested successfully.

### ACKNOWLEDGMENT

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